DAC/ADC Combination Finds Square Roots

Placing an A/D and D/A converter in the feedback loop of an op amp (**Figure 1**) forms a circuit whose output is proportional to the square root of applied voltages. The technique provides a bonus — you get the answer in digital form (from the A/D converter) in addition to the analog output at V_{OUT}. Output accuracy is better than 0.1% between -5V and -5mV, and the usuable dynamic range for V_{IN} extends more than five decades — down to -50µV. The circuit features 12-bit serial-interface converters.

The D/A converter (IC_2) generates an internal current (I_{DAC}) that represents the product of the applied digital code and the applied V_{REF} voltage: I_{DAC} equals the reference input current V_{REF}/R times the fraction D = code/2N, where R is an equivalent resistance for the internal R-2R ladder, and N is the converter's resolution in bits:

$$I_{DAC} = \left(\frac{V_{REF}}{R}\right) D .$$

Applying the same value to both inputs (V_{REF} and D) makes I_{DAC} correspond to the square of that value: $V_{REF} = V_{OUT}$ by direct connection, and D approximately equals $V_{OUT}/5V$ (the A/D converter's analog input divided by its full scale). Therefore, by substitution:

$$I_{DAC} \approx \left(\frac{V_{OUT}}{R}\right)\left(\frac{V_{OUT}}{5}\right) = \frac{V_{OUT}^2}{5R} .$$

Because feedback forces the summing junction to zero volts (see the simplified diagram within IC_2), I_{DAC} equals the input current $-V_{IN}/R$:

$$I_{DAC} = \frac{-V_{IN}}{R} \approx \frac{V_{OUT}^2}{5R}$$

$$\frac{V_{OUT}^2}{5} \approx -V_{IN}, \text{ therefore}$$

$$V_{OUT} \approx \sqrt{5}\sqrt{-V_{IN}} .$$

The $\sqrt{5}$ factor is associated with the A/D converter's 5V full-scale level, and affects the output as follows (you can remove this factor by changing the system gain):

V_{IN}	V_{OUT}
-5.000V	5.000V (full scale)
-1.250V	2.500V
-50mV	500mV
-0.5mV	50mV

IC_{4A} is a 1MHz oscillator that clocks the two converters. The A/D converter (IC_1) is configured for self starting and continuous conversions. Its CONVST output (pin 7) goes high after each conversion, causing IC_{4D} to deliver a $\overline{LOAD}$ pulse to the D/A converter.

Potentiometer R_4 adjusts full-scale, and R_5 provides an offset adjustment that improves the output accuracy for inputs between zero and -100mV. To calibrate the system, apply -5.000V at V_{IN} and adjust R_4 for 5.000V at V_{OUT}. Then apply -0.5mV at V_{IN} and adjust R_5 for 50.0mV at V_{OUT}.

Scope photos illustrate the circuit's DC behavior over the full range (**Figure 2a**) and near zero (**Figure 2b**). Zero volts for V_{IN} (the x axis) and V_{OUT} (the y axis) is at the lower right-hand corner of each photo. Note that **Figure 2b**, whose expanded scales reveal the A/D converter's quantizing steps, has the same parabolic shape as the full transfer function in **Figure 2a**. V_{OUT} exhibits a transient response of 80ms for V_{IN} in the range -1 to -5V. As V_{IN} approaches -10mV, the response slows to about 20ms.

To reduce the noise effects of digital coupling and 60Hz fields, you should shield the op amp's summing junction by minimizing connector lengths to that node (connections to IC_2, IC_3, and C_5) and by routing serial-interface lines away from the node.

(Circle 3)

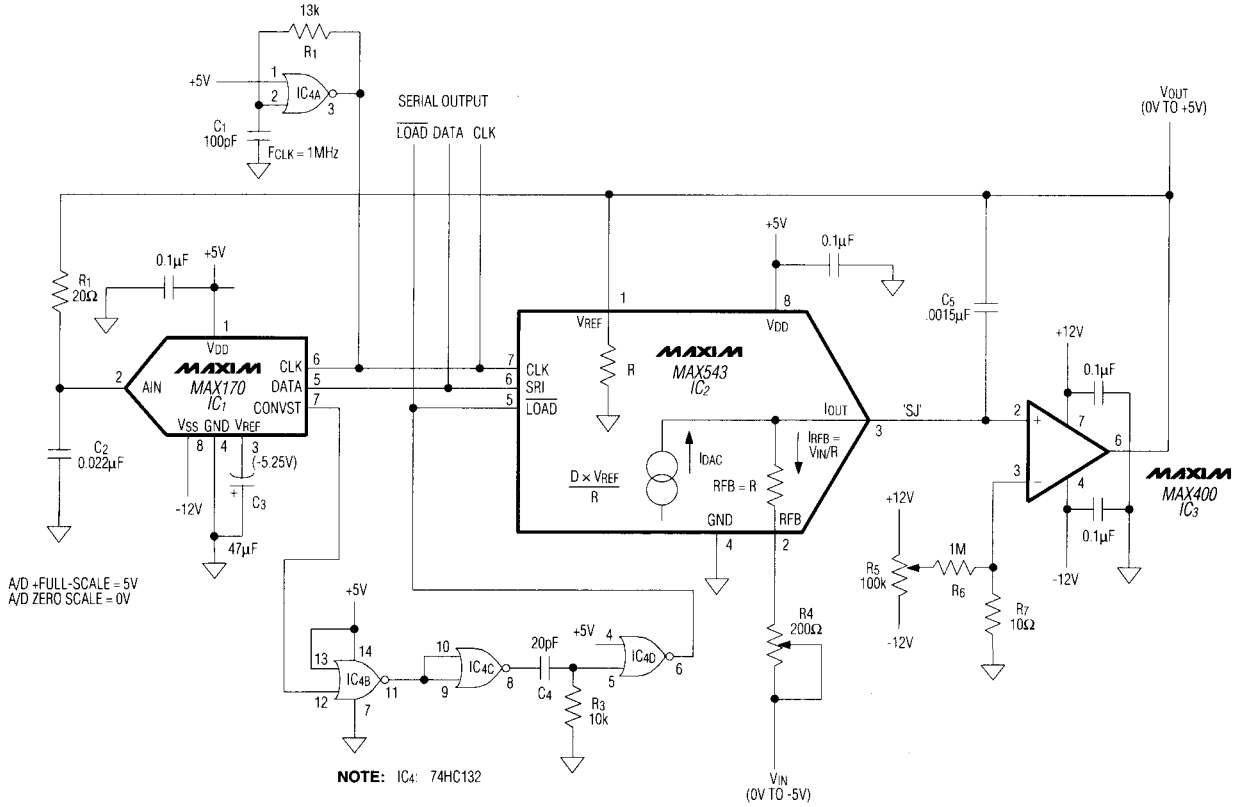
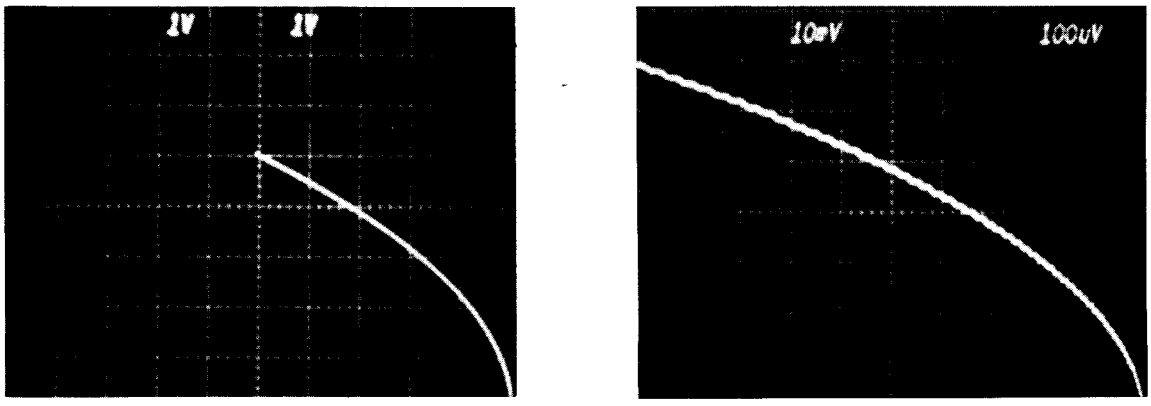


Figure 1. *The circuit generates, in analog and serial-digital form, an output proportional to the square root of voltages applied at* V_{IN}.



a.
VIN: x-AXIS, 1V/div
VOUT: y-AXIS, 1V/div

b.
VIN: x-AXIS, 100µV/div
VOUT: y-AXIS, 10mV/div

Figure 2. *These scope photos from Figure 1 show* V_{IN} *vs.* V_{OUT} *(*$V_{OUT} \approx \sqrt{5}\ \sqrt{-V_{IN}}$*) for the full input range (a) and for an expanded scale near zero (b).*